IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	)	
Sunay Tripathi et al.	)	Group Art Unit: 2443
	)	
Application No: 10/683,933	)	Examiner: Dennison, Jerry B
	)	
Filed: October 10, 2003	)	Atty. Docket No: Sunmp462
	)	
For: A SYSTEM AND METHOD FOR VERTICAL PERIMETER PROTECTION	)	Date: January 23, 2009

CERTIFICATE OF E-FILING

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office via electronic filing with EFS-Web on **January 23, 2009.**

Signed:_____/*Jayanthi Minisandram*/_____
Jayanthi Minisandram

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reasons stated below.

A Final Office Action was mailed October 24, 2008, indicating that the Amendment and Response to Office Action filed July 25, 2008, was not considered persuasive with regard to the 35 USC 102(e) rejections. Claims 1-8, 14, 19-20, 23-28, 33, 36-39, 41-51, 53-54 and 56-61 are pending in the application. Reconsideration of the present case is earnestly requested in light of the following remarks. Please note that for brevity, only the primary arguments directed to the independent claims are presented, and that additional arguments, e.g., directed to the subject matter of the dependent claims, may be presented if and when the case proceeds to Appeal.

ARGUMENT

Summary of Arguments

The Examiner's rejections are inappropriate for at least the following reasons:

Argument 1: Neither the DiMambro et al. (US Pat. No. 7,076,545) reference nor the Chang reference (U.S. Patent No. 6,338,078) teaches or suggests processing a packet associated with a connection through the plurality of protocol layers ***using a single thread from a single processor by assigning the connection to a single processor*** of a multiprocessor server system for processing wherein ***packets associated with the connection are directed to the single thread in the single processor;*** and

Argument 2: Further, neither the DiMambro reference nor the Chang reference teaches or even suggests ***preserving connection state information used by the plurality of protocol layers by mutual exclusion of other threads from processing packets for said connection through the plurality of protocol layers.***

Independent Claims 1, 20, 36, 44 and 53: Claims 1, 20, 36, 44 and 53 stand rejected under 35 U.S.C. 102(e) as being anticipated by DiMambro (U.S. Patent No. 7,076,545). In addition, independent claims 1, 20, 44, and 53 were rejected under 102(b) as being anticipated by Chang et al (U.S. Patent No. 6,338,078). The following clear errors in the Examiner's rejection are noted.

DiMambro discloses a method for load balancing the processing of received packets. Packets are received at a communication interface of a computer system and placed on a receive descriptor ring. An ISR (Interrupt Service Routine) or similar process retrieves packets from the ring and places the packet in one of a plurality of service queues which are tended by service threads or processes. DiMambro further teaches that retrieval of a packet from the receive descriptor ring is decoupled from the subsequent protocol related processing of the packet. This allows ISR to handle packets in shorter periods of time so that more packets can be handled in any given period of time. DiMambro asserts that by using multiple service queues and service threads to perform subsequent processing of the packets, efficient overall handling of received packets is enabled. (See DiMambro column 2, lines 35-44 and lines 47-57).

Chang describes a method of distributing input processing to multiple CPUs on multiprocessor systems to improve network throughput and take advantage of multiprocessor scalability. According to Chang, packets are received from the network and distributed to N high

priority threads, wherein N is the number of CPUs on the system. N queues are provided to which the incoming packets are distributed. When one of the queues is started, one of the threads is scheduled to process packets on this queue at any one of the CPUs that is available at the time. (See Abstract). The IP queue is concurrently processed by multiple threads with one thread per CPU, and one queue per thread. In this manner, the path length is shortened with more CPUs running parts of a packet's code simultaneously in a multithread fashion, thereby effecting the increased throughput. (See Column 5, lines 21-26). As in DiMambro, Chang teaches improving network throughput and using multiple threads to process packets of a connection.

Argument 1: Although DiMambro teaches that a packet may invoke functions or procedures for processing each protocol of a packet, DiMambro does not suggest or teach directing **all packets of a connection** to a single thread in a single processor for processing, as claimed by the instant application. In fact, the teachings of DiMambro are all directed to efficient load balancing during the processing of received packets and using multiple queues and threads to process packets.

Similarly, Chang does not suggest or teach directing **all packets of a connection** to a single thread in a single processor for processing, as claimed by the instant application. In fact, similar to DiMambro, Chang describes distributed input processing by assigning different packets to different queues. Chang mentions processing a packet by a thread but does not go beyond that to indicate that each packet of a connection is processed by a single queue of a single processor. By directing all packets of a connection to a single queue on a single processor, processing time is decreased by reducing data state conflicts between protocol layers. (See page 19, lines 16-21 of instant application).

Argument 2: Neither the DiMambro reference nor the Chang reference teach or even suggest preserving connection state information for a connection specific to a processor used by plurality of protocol layers at each processor for processing connection requests. The claimed invention preserves the connection state information by utilizing localized cache so that connection state information to process connection request is maintained locally so that data state conflicts between protocol layers can be reduced.

In contrast, the claimed invention preserves the connection state information specific to a processor within a localized cache associated with the processor of the multiprocessor server. This connection information is preserved by mutual exclusion of other threads. By preserving connection state information locally at each processor's localized cache, efficient processing of packets is enabled by reducing data state conflicts between protocol layers. The Examiner is relying

on Chang to teach preserving connection state information. However, the sections that the Examiner is relying on merely teaches engaging a hashing function to determine which queue/CPU pair each of the packets should be sent for processing. As different packets of a connection request may be routed and processed by different processors (See column 6, lines 30-32 of Chang), the connection state information of each processor is different and each of the packets are packaged with the related processors' distinct connection information. Further, due to different processors distinct protocols, data state conflicts may be encountered delaying the processing of the connection request. There is no mention of the packets being processed by a single processor with the connection state information of the specific processor being preserved locally by mutual exclusion of other threads so as to enable faster processing of packets for said connection.

As can be seen from the above, Applicant submits that the Office's insistence that DiMambro and Chang reference independently teach each and every element of the claimed invention is faulty as the references do not suggest or teach processing each of the packets of a connection through a single processor using a single thread nor suggest or teach preserving the connection state information for the processor by mutual exclusion of other threads.

Dependent Claims 2-8, 14, 19, 23-28, 33, 37-39, 41-43, 49-51, 54, 56-61:

Examiner relies on other references (Syvanne et al., US Pat. Pub. No. 2002/0112188 with regard to claims 6-8, 19, 23-26, 33, 37-39, 41-43, 49-51, and 56-59) in combination with Chang to correct the defects in Chang. However Applicant submits that, none of the cited references overcome the deficit of Chang as described above. Because a dependent claim incorporates each and every feature of its independent claim, the Applicant submits that each of dependent claims 2-8, 14, 19, 23-28, 33, 37-39, 41-43, 49-51, 54, 56-61 is patentable with respect to the cited art of record for at least the same reasons provided for its respective independent claims.

Conclusion

In view of the foregoing, the Applicant submits that the DiMambro or the Chang references or any of the other cited references whether considered alone or in any combination fail to teach or suggest each and every feature of each of independent claims 1, 20, 36, 44 and 53 and the corresponding dependent claims.

In view of the foregoing, the Applicant respectfully submits that all of the pending claims are in condition for allowance. The Applicant kindly requests that the Office withdraw the rejections of claims 1-8, 14, 19, 20, 23-28, 33, 36-39, 41-51, 53, 54 and 56-61, and issue a Notice of Allowance. If the Office has any questions concerning the present Request, the undersigned can be reached at (408) 774-6905. If any additional fees are due in connection with filing this Request, the

Commissioner is authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP462). Enclosed herewith is the associated Notice of Appeal.

Respectfully submitted,

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